PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Gregory Marlan et al. Examiner: Ryan A. Dare

Serial No.: 10/631,988 Group Art Unit: 2186

Filed: July 31, 2003 Docket: 499.750US1

For: DETECTION AND CONTROL OF RESOURCE CONGESTION BY A NUMBER OF PROCESSORS

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 18, 2006, from the Final Rejection of claims 1-40 of the above-identified application, as set forth in the Final Office Action mailed on April 18, 2006.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, SILICON GRAPHICS, INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on July 31, 2003 with 40 claims. In response to the Office Action mailed October 28, 2005, an Amendment was filed to amend claim 27 and 34-40. Claims 1-40 stand rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated April 18, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to, methods, systems and apparatus for detection and control of resource congestion by a number of processors. (See Figure 1).

In claim 1, an apparatus comprises a load/store unit that includes a retry logic that is to retry access to a resource after receipt of a negative acknowledgement for an attempt to access the resource by the load/store unit. (See the load/store functional unit 218 and the retry logic 286 in Figure 2 and page 15, line 27 – page 16, line 6). The apparatus also includes a congestion detection logic to output a signal that indicates that the resource is congested based on receipt of a consecutive number of negative acknowledgments in response to access requests to the resource. (See congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3).

In claim 5, a processor comprises a functional unit to attempt to access data from memory coupled to the processor based on an access request. (See the load/store functional unit 218 in Figure 2 and page 15, line 27 – page 16, line 6). The functional unit is to retry attempts to access of the data based on other access requests after receipt of a negative acknowledgement in response to the attempt to access the data. (See the load/store functional unit 218 in Figure 2 and page 15, line 27 – page 16, line 6). The processor also comprises a congestion detection logic to detect congestion of access of the data based on receipt of a consecutive number of negative acknowledgments that exceed a threshold prior to access of the data. (See the congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3). The processor comprises a congestion control logic to disable the functional unit from the attempts to access the data for a time period after congestion is detected. (See the congestion control logic 284 in Figure 2 and page 16, lines 7-13).

In claim 8, a processor comprises a functional unit to attempt to access a cache line in a cache memory coupled to the processor based on an access request. (See the processors 104 and the caches 102 in Figure 1 and page 13, lines 4-26). The functional unit is to retry attempts to access the cache line based on additional access requests after receipt of a negative acknowledgement in response to the attempt to access the data. (See the load/store functional unit 218 in Figure 2 and page 15, line 27 – page 16, line 6). The processor also comprises a

congestion detection logic to detect congestion of access of the cache line based on an average number of negative acknowledgments received that exceed a threshold prior to access of the data. (See the congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3). The processor comprises a congestion control logic to disable the functional unit from attempts to access the cache line for a time period after congestion is detected. (See the congestion control logic 284 in Figure 2 and page 16, lines 7-13).

In claim 12, a system comprises a cache memory to store data. (See the caches 102 in Figure 1 and page 12, lines 20-26). The system also comprises a first processor to attempt to access the data from the cache memory based on access requests. (See the processors 104 in Figure 1 and page 13, lines 4-26). The first processor includes a congestion detection logic to detect congestion of access to the data based on receipt of a consecutive number of negative acknowledgements in response to the access requests. (See the congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3).

In claim 17, a system comprises a resource. (See the caches 102 in Figure 1 and page 12, lines 20-26). The system also comprises a first processor having a load/store functional unit. (See the processor 104 and the load/store functional unit 218 in Figure 2 and page 15, lines 24-27). The load/store functional unit is to attempt to access the resource based on access requests. (See the load/store functional unit 218 in Figure 2 and page 15, line 27 – page 16, line 6). The first processor includes a congestion detection logic to detect congestion of access of the resource based on a consecutive number of negative acknowledgements received in response to the access requests prior to receipt of a positive acknowledgment in response to one of the access requests within a first time period. (See the congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3).

In claim 22, a system comprises a cache memory to include a number of cache lines for storage of data. (See the caches 102 in Figure 1 and page 12, lines 20-26). The system also comprises at least two processors, wherein a first processor of the at least two processors is to attempt to access the data in one of the number of cache lines based on access requests. (See the processors 104 in Figure 1 and page 13, lines 4-26). The first processor includes a congestion detection logic to detect congestion of access of a first cache line of the number of cache lines based on a ratio of a number of negative acknowledgments to a number of positive

acknowledgments received in response to the access requests. (See the congestion detection logic 282 in Figures 2 and 3 and page 16, line 24 – page 3).

In claim 27, a method comprises transmitting access requests, by a first processor, to access data in a memory. (See the block 702 in Figure 7 and page 20, lines 7-14). The method also comprises receiving a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests. (See the block 704 in Figure 7 and page 20, lines 15-22). The method comprises detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment. (See the block 710 in Figure 7 and page 21, lines 13-21; also see the block 912 in Figure 9 and page 24, line 25 – page 25, line 7).

In claim 31, a method comprises accessing, by at least one processor, a resource based on an access request. (See the block 902 in Figure 9 and page 23, lines 3-6). The method also comprises receiving a positive acknowledgement if the resource is accessible. (See the block 906 in Figure 9 and page 23, lines 7-15). The method comprises receiving a negative acknowledgement if the resource is not accessible. (See the block 906 in Figure 9 and page 23, lines 7-15). The method comprises retrying accessing, by the at least one processor, of the resource based on a number of access requests. (See the block 910 in Figure 9 and page 23, line 20 – page 24, line 24). The method also comprises detecting that a consecutive number of negative acknowledgements exceeds a first threshold within a time period, prior to receiving a positive acknowledgments. (See the block 910 in Figure 9 and page 23, line 20 – page 24, line 24).

In claim 34, a machine-readable medium provides instructions, which when executed by a machine, cause said machine to perform operations. (See page 11, lines 1-10). The operations comprise transmitting access requests, by a first processor, to access data in a memory. (See the block 702 in Figure 7 and page 20, lines 7-14). The operations also comprise receiving a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests. (See the block 704 in Figure 7 and page 20, lines 15-22). The operations also comprise detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative

acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment. (See the block 710 in Figure 7 and page 21, lines 13-21).

In claim 38, a machine-readable medium provides instructions, which when executed by a machine, cause said machine to perform operations. (See page 11, lines 1-10). The operations comprise accessing, by at least one processor, a resource based on an access request. (See the block 902 in Figure 9 and page 23, lines 3-6). The operations comprise receiving a positive acknowledgement if the resource is accessible. (See the block 906 in Figure 9 and page 23, lines 7-15). The operations also comprise receiving a negative acknowledgement if the resource is not accessible. (See the block 906 in Figure 9 and page 23, lines 7-15). The operations comprise retrying accessing, by the at least one processor, of the resource based on a number of access requests. (See the block 910 in Figure 9 and page 23, line 20 – page 24, line 24). The operations comprise detecting that a consecutive number of negative acknowledgements exceeds a first threshold within a time period, prior to receiving a positive acknowledgments. (See the block 910 in Figure 9 and page 23, line 20 – page 24, line 24).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5-6, 12-21, and 27-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes et al. (U.S. Patent No. 6,427,193) (hereinafter "Hughes") and Pitts et al. (U.S. Patent No. 4,893,248) (hereinafter "Pitts"). Claims 4 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Pitts as applied to claims 1-3, 5-6, 12-21, and 27-40, and further in view of "Enhancement of IEEE 802.11 Distributed Coordination Function with Exponential Increase Exponential Decrease Backoff Algorithm" by Nah-Oak Song et al. (hereinafter "Song"). Claims 8-10 and 22-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Aikawa et al. (U.S. Patent No. 6,898,751) (hereinafter "Aikawa"). Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Aikawa as applied to claims 8-10 and 22-26, and further in view of Song.

7. ARGUMENT

A) The Applicable Law for Rejection under 35 U.S.C. § 103

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness.[1] To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references.[2]

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."[3]

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.[4]

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference.[5] At the same time, however, although it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings

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[1] *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).
[2] *Id.*
[3] *Id.* (emphasis in original).
[4] *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).
[5] *In re Oetiker*, 24 USPQ2d 1443 (Fed. Cir. 1992).

and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching.[6] The references must teach or suggest all the claim elements.[7]

B) Discussion of the rejection of claims 1-3, 5-6, 12-21, and 27-40 under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Pitts.

No Motivation to Combine the References: With regard to claims 1-3, 5-6, 12-21, and 27-40, Applicant submits that the Office Action does not identify any teachings of the prior art or knowledge of ordinary skill in the art that would motivate one to modify Hughes using Pitts. In the Response to Arguments section of the Final Office Action, the Office indicated that "[s]ince each reference seeks to solve a similar problem, a skilled artisan would have been motivated to combine the references at the time the invention was made."[8]

Applicant respectfully traverses this assertion. First, the cited references are nonanalogous art. Hughes relates to "load/store units within processors."[9] Pitts relates to remote terminals and a central terminal "which monitors and accumulates data for pay for view television programs . . ."[10] Thus, Hughes relates to the multi-processor technology, while Pitts relates to data monitoring/accumulation technology for pay-per-view programming. Furthermore, the cited references solve different problems. Hughes solves a problem related to deadlocking in a multi-processor environment. Pitts solves a problem related to reporting of data from remote terminals for pay per view program. Thus, the references are not solving a similar problem. Thus, the Office Action has not established a *prima facie* case of obviousness under 35 U.S.C. §103.

Combining the References Does Not Teach All Limitations:

Claims 1-4, 6, 12-21, 27-30 and 34-37

[6] (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979)).
[7] M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).
[8] Final Office Action at ¶63.
[9] Hughes at column 1, lines 6-7.
[10] Pitts at column 1, lines 7-17.

With regard to claim 1, among the differences, claim 1 recites "a congestion detection logic to output a signal that indicates that the resource is congested based on receipt of a consecutive number of negative acknowledgments in response to access requests to the resource." In the Advisory Action, the Office indicated the following:

> The contents of the report message are unimportant, as a report message is only generated if the resource is shown to be congested. Even though Pitts does not mention the word "congestion" specifically, it is clear that Pitts relates to congestion of a resource (see page 21, numerical 65 of the Final Office Action).[11]

Applicant respectfully traverses this assertion. The report message provides no indication of congestion (regardless of whether the message is considered a signal). A report message includes "data indicative of the authorized program(s) and the identity code of the remote terminal to the central station."[12] The report message is sent from a remote terminal 10 to a central station 11. A non-acknowledgement signal (NAK) is transmitted from the central station 11 to the remote terminal 10 if a "parity check" is not validated based on a block sum check. In other words, a NAK is transmitted back to the remote terminal 10 is the substantive data of the report message has been corrupted during the transmission from the remote terminal 10 to the central station 11. After three NAKs are received, the NAK counter is zeroed out and the report message is again transmitted.[13] Therefore, Applicant respectfully disagrees that Pitts discloses that the report message is generated if there is congestion. Pitts relates to repeatedly transmitting of a report message because of parity check invalidity (corruption of the data in the message); not because of congestion at the central station 10.

Thus, the cited references do not disclose or suggest all of the claim limitations. Accordingly, Applicant respectfully submits that the rejection of claim 1 under 35 U.S.C. §103 has been overcome. Because claims 2-3 depend from and further define claim 1, Applicant respectfully submits that the rejection of claims 2-3 has been overcome for at least the same reason.

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[11] Advisory Action at page 2.
[12] Pitts at column 2, line 68- column 3, line 2.
[13] See Pitts at column 21, lines 35-40.

With regard to claim 5, among the differences, claim 5 recites "a congestion detection logic to detect congestion of access of the data based on receipt of a consecutive number of negative acknowledgments that exceed a threshold prior to access of the data." Based on the remarks set forth above regarding claim 1, Applicant respectfully submits that the cited references do not disclose or suggest all of the claim limitations. Therefore, Applicant respectfully submits that the rejection of claim 5 under 35 U.S.C. §103 has been overcome. Because claim 6 depends from and further defines claim 5, Applicant respectfully submits that the rejection of claim 6 has been overcome for at least the same reason.

With regard to claim 12, among the differences, claim 12 recites "wherein the first processor includes a congestion detection logic to detect congestion of access to the data based on receipt of a consecutive number of negative acknowledgements in response to the access requests." Based on the remarks set forth above regarding claim 1, Applicant respectfully submits that the cited references do not disclose or suggest all of the claim limitations. Therefore, Applicant respectfully submits that the rejection of claim 12 under 35 U.S.C. §103 has been overcome. Because claims 13-16 depends from and further define claim 12, Applicant respectfully submits that the rejection of claims 13-16 has been overcome for at least the same reason.

With regard to claim 17, among the differences, claim 17 recites "a congestion detection logic to detect congestion of access of the resource based on a consecutive number of negative acknowledgements received in response to the access requests prior to receipt of a positive acknowledgment in response to one of the access requests within a first time period." In the Response to Arguments section of the Final Office action, the Office reiterated its position that Pitts at column 21, lines 24-40 "teaches sending a signal and zeroing the counter after a number of negative acknowledgements, specifically three."[14] The Office also referenced Pitts at column 23, lines 1-13 for support that Pitts teaches congestion. Neither section of Pitts discloses or suggests that there is congestion detected if a number of negative acknowledgements are received in a given time period. Accordingly, Applicant respectfully submits that the rejection of claim 17 under 35 U.S.C. §103 has been overcome. Because claims 18-21 depend from and

[14] Final Office Action at ¶65.

further define claim 17, Applicant respectfully submits that the rejection of claims 18-21 has been overcome for at least the same reason.

With regard to claims 27 and 34, Applicant respectfully submits that such claims are patentable for at least the reasons set forth above regarding claims 1 and 17. Because claims 28-30 and 35-37 depend from and further define claims 27 and 34, respectively, Applicant respectfully submits that the rejection of claims 28-30 and 35-37 has been overcome for at least the same reason.

With regard to claims 31 and 38, Applicant respectfully submits that such claims are patentable for at least the reasons set forth above regarding claims 1 and 17. Because claims 32-33 and 39-40 depend from and further define claims 31 and 38, respectively, Applicant respectfully submits that the rejection of claims 32-33 and 39-40 has been overcome for at least the same reason.

C) Discussion of the rejection of claims 4-7 under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Pitts and in further view of Song.

In addition to the remarks set forth above regarding claims 1 and 5 from which claims 4 and 7 depend respectively, Applicant respectfully submits the following remarks. Applicant submits that the Office Action does not identify any teachings of the prior art or knowledge of ordinary skill in the art that would motivate one to modify Hughes using Pitts and using Song. In the Response to Arguments section of the Final Office Action, the Office indicated that the Abstract of Song provides the suggestion to combine.[15] Applicant respectfully traverses this assertion. Song relates to backoff algorithms for a wireless communication standard – IEEE 802.11. Hughes relates to "load/store units within processors."[16] Pitts relates to remote terminals and a central terminal "which monitors and accumulates data for pay for view television programs . . ."[17] The abstract in Song does not provide any suggestion that the algorithms for a wireless communication standard can be combined with load/store units within processors or with data accumulation for pay for view programs. Thus, the Office Action has

[15] Final Office Action at ¶68.
[16] Hughes at column 1, lines 6-7.
[17] Pitts at column 1, lines 7-17.

not established a *prima facie* case of obviousness under 35 U.S.C. §103. Thus, the Office Action has not established a *prima facie* case of obviousness under 35 U.S.C. §103 for claims 4 and 7.

D) Discussion of the rejection of claims 8-10 and 22-26 under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Aikawa.

No Motivation to Combine the References: With regard to claims 8-10 and 22-26, Applicant submits that the Office Action does not identify any teachings of the prior art or knowledge of ordinary skill in the art that would motivate one to modify Hughes using Aikawa. In the Response to Arguments section of the Final Office Action, the Office indicated that "both Hughes and Aikawa teach systems that aim to reduce congestion."[18] Applicant respectfully traverses this assertion. As previously discussed, Hughes solves a problem related to deadlocking in a multi-processor environment. Aikawa solves a problem related to polling among computing systems. These references are not solving a similar problem. Moreover, neither reference even uses the term "congestion." Therefore, there is no motivation to combine such references. Thus, with regard to claims 8-10 and 22-26, the Office Action has not established a *prima facie* case of obviousness under 35 U.S.C. §103.

Combining the References Does Not Teach All Limitations: Moreover, with regard to claims 22-26, Applicant submits that the combining of the cited references does not teach all of the claimed limitations.

Among the differences, claim 22 recites "a congestion detection logic to detect congestion of access of a first cache line of the number of cache lines based on a ratio of a number of negative acknowledgments to a number of positive acknowledgments received in response to the access requests." In the Response to Arguments section of the Final Office Action, the Office indicated "Aikawa mentions the use of ACKs in addition to NAKs."[19] As noted in Applicant's prior response, the section cited by the Office (regarding the use of a ratio

[18] Final Office Action at ¶69.
[19] Final Office Action at ¶70.

of NAKs to ACKs) does NOT disclose ACKs. Further, this section does not disclose a ratio of NAKs to ACKs.

In the Response to Arguments section of the Final Office Action, the Office further indicated the following:

> While the Aikawa reference does not anticipate all limitations of claim 22, it has been shown above that the combination of Aikawa and Hughes would allow the skilled artisan to have a good chance of success in achieving the invention of claim 22.[20]

In other words, none of the cited references disclose the claimed limitations. Applicant notes for the record that the Examiner appears to taking official notice of the missing elements, which is timely traversed herein under M.P.E.P. § 2144.03, and if the Examiner is aware of a reference providing support for the assertion, citation of such reference is respectfully requested. If a reference cannot be provided, Applicant submits the assertion is formed on personal knowledge and Applicant requests that an affidavit be provided, as required by 37 C.F.R. § 1.104(d), or withdrawal of this 35 U.S.C. § 103 rejection. Because claims 23-26 depend from and further define claim 22, Applicant respectfully submits that the rejection of claims 23-26 has been overcome for at least the same reason.

E) Discussion of the rejection of claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Hughes and Aikawa and further in view of Song.

In addition to the remarks set forth above regarding claim 8 from which claim 11 depends, Applicant respectfully submits the following remarks. With regard to claim 11, Applicant submits that the Office Action does not identify any teachings of the prior art or knowledge of ordinary skill in the art that would motivate one to modify Hughes using Aikawa and Song.

In the Response to Arguments section of the Final Office Action, the Office indicated that the Abstract of Song provides the suggestion to combine.[21] Applicant respectfully traverses this assertion. Song relates to backoff algorithms for a wireless communication standard – IEEE

[20] Final Office Action at ¶70.
[21] Final Office Action at ¶68.

802.11. Hughes relates to "load/store units within processors."[22] Aikawa relates to polling among computing systems.[23] The abstract in Song does not provide any suggestion that the algorithms for a wireless communication standard can be combined with load/store units within processors or with polling among computing systems. Thus, the Office Action has not established a *prima facie* case of obviousness under 35 U.S.C. §103. Thus, the Office Action has not established a *prima facie* case of obviousness under 35 U.S.C. §103 for claim 11.

[22] Hughes at column 1, lines 6-7.
[23] Aikawa at column 1, lines 8-10.

8. SUMMARY

It is respectfully submitted that the claims are patentable over the cited art. Reversal of the rejection and allowance of the pending claim are respectfully requested.

Respectfully submitted,

GREGORY MARLAN et al.

By their Representatives,

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LISA POSARSKE
Name

Signature

CLAIMS APPENDIX

1. An apparatus comprising:

a load/store unit that includes a retry logic that is to retry access to a resource after receipt of a negative acknowledgement for an attempt to access the resource by the load/store unit; and

a congestion detection logic to output a signal that indicates that the resource is congested based on receipt of a consecutive number of negative acknowledgments in response to access requests to the resource.

2. The apparatus of claim 1 further comprising a congestion control logic to disable the retry logic from retry accesses to the resource based on receipt of the signal from the congestion detection logic.

3. The apparatus of claim 2, wherein the congestion control logic is to exponentially increase the delay after the congestion detection logic is to detect congestion while the resource is currently congested.

4. The apparatus of claim 2, wherein the congestion control logic is to exponentially decrease the delay after the congestion detection logic receive a number of positive acknowledgements in response to access requests to the resource.

5. A processor comprising:

a functional unit to attempt to access data from memory coupled to the processor based on an access request, wherein the functional unit is to retry attempts to access of the data based on other access requests after receipt of a negative acknowledgement in response to the attempt to access the data; and

a congestion detection logic to detect congestion of access of the data based on receipt of a consecutive number of negative acknowledgments that exceed a threshold prior to access of the data; and

a congestion control logic to disable the functional unit from the attempts to access the data for a time period after congestion is detected.

6. The processor of claim 5, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access to other data in the memory is congested.

7. The processor of claim 6, wherein the congestion control logic is to exponentially decrease the time period after the congestion detection logic receives a number of positive acknowledgements in response to attempts to access data in the memory.

8. A processor comprising:

a functional unit to attempt to access a cache line in a cache memory coupled to the processor based on an access request, wherein the functional unit is to retry attempts to access the cache line based on additional access requests after receipt of a negative acknowledgement in response to the attempt to access the data;

a congestion detection logic to detect congestion of access of the cache line based on an average number of negative acknowledgments received that exceed a threshold prior to access of the data; and

a congestion control logic to disable the functional unit from attempts to access the cache line for a time period after congestion is detected.

9. The processor of claim 8, wherein the average number of negative acknowledgements is within a window and wherein the congestion detection logic is to move the window over time of attempts to access the cache line by the functional unit.

10. The processor of claim 8, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access of other cache lines in the cache memory is congested.

11. The processor of claim 8, wherein the congestion control logic is to exponentially decrease the time period after the congestion detection logic receives a number of positive acknowledgements in response to attempts to access other cache lines in the cache memory.

12. A system comprising:

a cache memory to store data; and

a first processor to attempt to access the data from the cache memory based on access requests, wherein the first processor includes a congestion detection logic to detect congestion of access to the data based on receipt of a consecutive number of negative acknowledgements in response to the access requests.

13. The system of claim 12 further comprising:

a second processor associated with the cache memory;

a hub controller to receive the access requests from the first processor, the hub controller to forward the access requests to the second processor, wherein the second processor is to determine whether the data in the cache memory is accessible.

14. The system of claim 13, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the data is not accessible, the second processor to transmit a positive acknowledgment back to the first processor through the hub controller if the data is accessible.

15. The system of claim 12, wherein the first processor further comprises a congestion control logic to disable the first processor from transmitting the access requests if the congestion detection logic determines that access to the data is congested.

16. The system of claim 12, wherein the congestion control logic is to disable the first processor from transmitting the access requests for a time period, wherein the time period is based on an exponential back off delay operation.

17. A system comprising:

a resource; and

a first processor having a load/store functional unit, the load/store functional unit to attempt to access the resource based on access requests, wherein the first processor includes a congestion detection logic to detect congestion of access of the resource based on a consecutive number of negative acknowledgements received in response to the access requests prior to receipt of a positive acknowledgment in response to one of the access requests within a first time period.

18. The system of claim 17 further comprising:

a second processor associated with the resource;

a hub controller to receive the access requests from the first processor, the hub controller to forward the access requests to the second processor, wherein the second processor is to determine whether the resource is accessible.

19. The system of claim 18, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the resource is not accessible, the second processor to transmit a positive acknowledgment back to the first processor through the hub controller if the resource is accessible.

20. The system of claim 17, wherein the first processor further comprises a congestion control logic to disable the load/store functional unit from attempting to access the resource if the congestion detection logic is to detect congestion of access of the resource

21. The system of claim 17, wherein the congestion control logic is to disable the load/store unit from attempts to access the resource for a second time period, wherein the second time period is based on an exponential back off delay operation.

22. A system comprising:

a cache memory to include a number of cache lines for storage of data; and

at least two processors, wherein a first processor of the at least two processors is to attempt to access the data in one of the number of cache lines based on access requests, wherein the first processor includes a congestion detection logic to detect congestion of access of a first cache line of the number of cache lines based on a ratio of a number of negative acknowledgments to a number of positive acknowledgments received in response to the access requests.

23. The system of claim 22, wherein a second processor of the at least two processors is associated with the cache memory and wherein the system further comprises a hub controller, the hub controller to receive the access requests from the first processor, the hub controller to forward the access requests to the second processor, wherein the second processor is to determine whether the one of the number of cache lines is accessible.

24. The system of claim 23, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the one of the number of cache lines is not accessible, the second processor to transmit a positive acknowledgement back to the first processor through the hub controller if the one of the number of cache lines is accessible.

25. The system of claim 22, wherein the first processor further comprises a congestion control logic to disable, for a time period, the first processor to attempt to access the data if the congestion detection logic is to detect congestion of access of the first cache line.

26. The system of claim 25, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access to other cache lines in the cache memory.

27. A method comprising:

transmitting access requests, by a first processor, to access data in a memory;

receiving, by the first processor, a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests; and

detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment.

28. The method of claim 27 further comprising controlling access to the data in the memory if the consecutive number of negative acknowledgements, received by the first processor, exceeds the first threshold, prior to receipt of the positive acknowledgement.

29. The method of claim 28, wherein controlling access to the data in the memory comprises disabling transmitting of the access requests, by the first processor, for a time period.

30. The method of claim 29, wherein controlling access to the resource comprises exponentially increasing the time period upon determining that the congestion is detected for other data in the memory while the time period has not expired.

31. A method comprising:

accessing, by at least one processor, a resource based on an access request;

receiving a positive acknowledgement if the resource is accessible;

receiving a negative acknowledgement if the resource is not accessible;

retrying accessing, by the at least one processor, of the resource based on a number of access requests; and

detecting that a consecutive number of negative acknowledgements exceeds a first threshold within a time period, prior to receiving a positive acknowledgments.

32. The method of claim 31 further comprising controlling access to the resource if the consecutive number of negative acknowledgements, received by the at least one processor, exceeds the first threshold, prior to receipt of the positive acknowledgement.

33. The method of claim 31, wherein controlling access to the resource comprises disabling transmitting of the access requests, by the first processor, for a time period.

34. A computer storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

transmitting access requests, by a first processor, to access data in a memory;

receiving, by the first processor, a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests; and

detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment.

35. The computer storage medium of claim 34 further comprising controlling access to the data in the memory if the consecutive number of negative acknowledgements, received by the first processor, exceeds the first threshold, prior to receipt of the positive acknowledgement.

36. The computer storage medium of claim 35, wherein controlling access to the data in the memory comprises disabling transmitting of the access requests, by the first processor, for a time period.

37. The computer storage medium of claim 36, wherein controlling access to the resource comprises exponentially increasing the time period upon determining that the congestion is detected for other data in the memory while the time period has not expired.

38. A computer storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

accessing, by at least one processor, a resource based on an access request;

receiving a positive acknowledgement if the resource is accessible;

receiving a negative acknowledgement if the resource is not accessible;

retrying accessing, by the at least one processor, of the resource based on a number of access requests; and

detecting that a consecutive number of negative acknowledgements exceeds a first threshold within a time period, prior to receiving a positive acknowledgments.

39. The computer storage medium of claim 38 further comprising controlling access to the resource if the consecutive number of negative acknowledgements, received by the at least one processor, exceeds the first threshold, prior to receipt of the positive acknowledgement.

40. The computer storage medium of claim 39, wherein controlling access to the resource comprises disabling transmitting of the access requests, by the first processor, for a time period.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.